The drawings were objected to for not showing every feature of the claimed invention. New Figures 3, 4, and 5 are proposed herein in response to the objection.

Claims 2, 4, 15, and 17 stand rejected under 35 U.S.C. 112, first paragraph. The claims have been amended in response to the rejection.

Claims 2 and 12 stand rejected under 35 U.S.C. 112, second paragraph. The claims have been amended in response to the rejection.

Claim 1 stands rejected under 35 U.S.C. 102(b) as being anticipated by Yamasaki, et al. (U.S. Patent No. 5,973,554). Claim 1 includes the feature of "a network of power distribution lines deposited on the surface of said chip, located directly over active components of said circuit." Yamasaki does not disclose such a feature. Note that element 70 in Yamasaki's Figures 2B and 3 is a capacitor, not an active component. Therefore, Applicant respectfully submits that Claim 1 is patentable over Yamasaki.

Claims 2-6, 8-10, 12-16, 18 and 19 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki in view of Tani (U.S. Patent No. 5, 468,993). Claim 2 includes the feature of "electrically conductive films deposited on said overcoat and patterned into a network of lines substantially vertically over said active components." As noted above, Yamasaki does not disclose or suggest such a feature. Yamasaki's element 70 is a capacitor, not an active component. In addition, Claim 2 includes the feature of "electrically conductive films deposited on said overcoat and patterned into a network of lines substantially vertically over said active components, said films in contact with said vias and having at least one stress-absorbing film and an outermost film being non-corrodible and metallurgically attachable." Yamasaki does not disclose or suggest a stress-absorbing film. Both of Yamasaki's layers 4 and 5

are aluminum. Further, Claim 2 includes the feature of "a leadframe having a chip mount pad, a first plurality of segments providing electrical signals, and a second plurality of segments providing electrical power and ground." Yamasaki's leadframe 2, 61 is a so-called "lead-on-chip" style in which no die mount pad is used. Tani is therefore nonanalogous art and one skilled in the art would receive no motivation from the cited references for a combination of Tani's traditional leadframe die mount pad with that of Yamasaki's lead-on-chip style leadframe. Claims 3-6, 8-10, 12-16, 18, and 19 depend from Claim 2 and are therefore patentable over the cited references for at least the reasons presented above.

Claim 7 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki in view of Tani in view of Applicant's Admitted Prior Art. Claim 7 depends from Claim 2, which as indicated above, is patentable over Yamasaki in view of Tani. Applicant's Admitted Prior Art does not cure the deficiencies of Yamasaki and Tani with respect to Claim 2. Therefore, Applicant respectfully submits that Claim 7 is patentable over the references of record for at least the reasons presented above. Additionally, Claim 7 has been amended to clarify that it is a structure claim.

Claims 11, 15, and 17 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yamasaki in view of Tani in view of Wolf. Claims 11, 15, and 17 depend from Claim 2, which as indicated above, is patentable over Yamasaki in view of Tani. Wolf does not cure the deficiencies of Yamasaki and Tani with respect to Claim 2. Therefore, Applicant respectfully submits that Claims 11, 15, and 17 are patentable over the references of record for at least the reasons presented above.

Applicant respectfully requests reconsideration and withdrawal of the rejections and allowance of Claims 1-3 and 5-19. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

In the Section titled "BRIEF DESCRIPTION OF THE DRAWINGS":

-- FIG. 1 is a simplified and schematic perspective view of a portion of an integrated circuit chip having bonding wires attached to bond pads and connected to portions of a leadframe, according to prior art.

FIG. 2 is a simplified and schematic perspective view of a portion of an integrated circuit chip having a surface structure integrating the power distribution functions of circuit and leadframe, according to the invention.

<u>FIG. 3 is a version of the perspective view of FIG. 2 showing detail of the power distribution lines.</u>

<u>FIG. 4 shows the use of solder balls as connections to the power distribution lines.</u>

<u>FIG. 5 shows the integrated circuit chip and power distribution lines relative to the leadframe upon which the chip is mounted.</u> --

On page 14, in the first full paragraph:

-- FIG. 2 summarizes the innovations of the present invention in order to remedy the above-listed shortcomings of the known technology. FIG. 2 is a simplified and schematic perspective view of a portion of an IC chip, generally designated 200, with design and fabrication features disclosed by the present invention. Semiconductor substrate 201 has a first ("active") surface 201a and a second ("passive") surface 201b. The second surface 201b is attached to the chip mount pad (<u>221 in FIG. 3 and FIG. 5</u> [not shown in FIG. 2]) of a prefabricated leadframe (typically copper, copper alloy, iron-nickel alloy, invar, or aluminum, about 100 to 300 μm thick). Of the plurality of leads (usually 14 up to over 600), FIG. 2 depicts only the tips 220a and 220b of a few leadframe segments, which are employed for power supply and located in the proximity of

the IC chip. FIG. 5 shows a plan view of the leadframe 500 with the IC chip 502 mounted on the chip mount pad 221. --

On page 16, in the second paragraph:

-- The outermost metal 271 of the deposited lines 251 and 252 is selected from a material which is bondable (and solderable, see below). Electrical conductors (506 in FIG. 5) connect this outermost metal with the lead tips (504 in FIG. 5) of the leadframe. In FIG. 2, wire bonding (the wire is preferably pure or alloyed gold, copper, or aluminum with a diameter of about 20 to 30 μm) is chosen as the preferred technique for electrical interconnection. Balls 208 and 209 are attached to lines 251 and 252, respectively, and stitches 210 and 211 are attached to lead tips 220a and 220b, respectively. It is important for the present invention that recent technical advances in wire bonding now allow the formation of tightly controlled wire loops and loop shapes. By way of example, loop 240 in FIG. 2 is shown much more elongated than loop 241. Wire lengths of 7.5 mm or even more are achievable with today's bonders. Such advances can, for instance, be found in the computerized bonder 8020 by Kulicke & Soffa, Willow Grove, PA, U.S.A., or in the ABACUS SA by Texas Instruments, Dallas, TX, U.S.A. Moving the capillary in a predetermined and computer-controlled manner through the air will create a wire looping of exactly defined shape. For instance, rounded, trapezoidal, linear and customized loop paths can be formed. --

On page 17, in the first paragraph:

-- The preferred structure of the deposited power distribution metallization for lines 251 and 252 consists of a seed metal layer (272 in FIG. 3) attached to the protective overcoat 230 and the bottoms of the vias 260, followed by a first relatively thin stress-absorbing metal layer (273 in FIG. 3), a second, relatively thick stress absorbing layer (274 in FIG. 3), and finally an outermost bondable metal layer (271 in FIG. 3). Preferably, the seed metal layer is selected from a group consisting of tungsten, titanium, titanium nitride, molybdenum, chromium,

and alloys thereof. The seed metal layer is electrically conductive, provides adhesion to both the metallization of the IC active components and the protective overcoat, permits the exposed portions of its upper surface to be electroplated, and prevents migration of the subsequent stress-absorbing metals to the components metallization layers. The thickness of seed metal layer is between about 100 and 500 nm. Alternatively, the seed metal layer may be composed of two metal layers; an example for the second metal is copper, since it provides a suitable surface for subsequent electroplating. --

On page 19, in the second paragraph:

-- As pointed out above, the outermost line layer may be selected so that it is solderable. A solder ball can then be attached to it by standard reflow techniques. However, it was described in the above-cited U.S. Patent Applications # 09/611,623 and 60/221,051 that it is often advisable to employ an additional solder mask (400 shown in FIG. 4) or polyimide layer with an opening (402) for each solder ball (404) in order to keep the flip-chip bump in a defined area and shape during bump formation and subsequent attachment to an external package or board. --

On page 20, in the first paragraph:

For operating the signal inputs/outputs of the IC, additional windows in the protective overcoat are needed to expose the underlying contact pad metallization (508 in FIG. 5). Wire bond (510 in FIG. 5) or solder balls can then be affixed to these contact windows. These windows and their respective wire bonds are not shown in FIG. 2.

In the Claims:

2. (amended) A semiconductor device having an additional conductor network on the chip surface, wherein the power distribution of the integrated circuit is combined with the power distribution of the leadframe, comprising:

a semiconductor chip having first and second surfaces;

an integrated circuit fabricated on said first chip surface, said circuit having active components, <u>contact pads,</u> at least one metal layer, and being protected by a mechanically strong, electrically insulating overcoat having a plurality of metal-filled vias to contact said at least one metal layer[, and a plurality of windows to expose circuit contact pads];

electrically conductive films deposited on said overcoat and patterned into a network of lines substantially vertically over said active components, said films in contact with said vias and having at least one stress-absorbing film and an outermost film being non-corrodible and metallurgically attachable;

said network patterned to distribute power current and ground potential;

a leadframe having a chip mount pad, a first plurality of segments providing electrical signals, and a second plurality of segments providing electrical power and ground;

said second chip surface attached to said chip mount pad;

electrical conductors connecting said [chip] contact pads with said first plurality of segments; and

electrical conductors connecting said network lines with said second plurality of segments.

4. (cancelled)

7. (amended) The device according to Claim 2 wherein said leadframe <u>comprises</u> [is pre-fabricated from] a sheet-like material selected from a group consisting of copper, copper alloy, aluminum, iron-nickel alloy, or invar.

10. (amended) The device according to Claim 8 wherein leadframe segment portions not included in said encapsulation are shaped as leads [or pins,] solderable to outside parts.

11. (amended) The device according to Claim 2 further comprising solder balls attached to said electrical conductors connecting said network lines with said second plurality of segments [wherein said lines and contact pads are attached to outside parts by solder balls].

12. (amended) The device according to Claim 2 further comprising a wire bond to said electrical conductors connecting said network lines with said second plurality of segments [wherein said metallurgical attachment comprises wire ball and stitch bonding, ribbon bonding, and soldering].

15. (amended) The device according to Claim 2 wherein said conductors are bonding wires [, bonding ribbons,] or solder balls.